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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/824,401 | 04/15/2004 | Du-Yeul Kim | SEC.1146 | 6396 |

20987 7590 03/17/2009

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|---|---|
| SAVLA, ARPAN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2185 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 03/17/2009 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/824,401 | KIM, DU-YEUL | |
| | Examiner | Art Unit | |
| | Arpan P. Savla | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-6,8-14 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 5* is/are allowed.

6)☒ Claim(s) *1-3,6,8-14 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

This Office action is in response to Applicant's communication filed December 4, 2008 in response to the Office action dated April 9, 2008. Claims 1-10, 12, and 14 have been amended. Claims 7, 15, and 16 have been canceled. New claim 17 has been added. Claims 1-6, 8-14, and 17 are pending in this application.

## OBJECTIONS

### *Claims*

1. In view of Applicant's amendment, the objections to **claims 1, 6, and 7** are withdrawn.

2. **Claim 8** is objected to because the phrase "method of claim **7**" should instead read "method of claim **6**" because claim 7 is now canceled.

## REJECTIONS NOT BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. **Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to**

**reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.**

As an initial matter, it must not be forgotten that claim 13 incorporate all the limitations of claim 12. As currently amended, claim 12 recites each pulse of the first control pulse signal is delayed relative to each pulse of the clock signal by a first delay and each pulse of the second control pulse is delayed relative to each pulse of the clock signal by a second delay. (emphasis added) Turning to Fig. 7 of Applicant's drawings, the pulse of PCLK ("clock signal") that goes high during time period C0 (i.e. the initial pulse of PCLK) would be supported by the claim language "each pulse of the clock signal." Also, the pulse of FRP ("first control pulse signal") that goes high during time period C1 (i.e. the initial pulse of FRP) would be supported by the claim language "each pulse of the first control pulse signal." Finally, the pulse of SRP ("second control pulse signal") that goes high during time period C1 (i.e. the initial pulse of SRP) would be supported by the claim language "each pulse of the second control pulse signal."

The Examiner now submits this example of Applicant's invention. The time from the initial PLCK going high until the initial FRP going high is measured by a first delay (the left-most arrow in Fig. 7). The time from the initial PLCK going high until the initial SRP going high is measured by a second delay. It is very important to note that this example provided by the Examiner is fully supported by the current language of claim 12. In this example, under no circumstances can the second delay be larger than the first delay. Accordingly, claim 13 contains subject matter which was not described in

the specification and therefore the Examiner maintains the 112, first paragraph rejection of claim 13.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

As detailed in the 112, first paragraph rejection above, in the example provided by the Examiner, under no circumstances can the second delay be larger than the first delay. Accordingly, the limitation "the first delay is larger than the second delay" is vague and indefinite and therefore the Examiner maintains the 112, second paragraph rejection of claim 13.

## REJECTIONS BASED ON PRIOR ART

### *Claim Rejections - 35 USC § 103*

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**8. Claims 1-3, 6, 8-10, 12, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda (U.S. Patent 6,363,465) (hereinafter "Toda-465") in view of Nam (U.S. Patent 6,633,995).**

9. **As per claim 1**, Toda-465 discloses a pipeline memory device comprising:

a plurality of memory cells that store data (col. 10, lines 45-46; Fig. 2, element 12);

a data transfer path on which the data is transferred (col. 10, lines 38-41; Fig. 1);

a data fetching control circuit (col. 10, lines 50-54; Fig. 2, element 24) configured to generate a first pipeline control pulse signal (col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements "CLK/CLK0" and "CK0"); *It should that the external clock signal "CLK/CLK0" is analogous to the "first clock signal" and "CK0" is analogous to the "first pipeline control signal." It should also be noted that when taking the circuits from Figs. 18A and 18B and using those circuits to generate "CK0" as illustrated in Figs. 19A and 19B, the signal "P1" is always high and the signal "CK0" is a don't care, as explained in col. 20, line 63 - col. 21, line 3.*

and a second pipeline control pulse signal (col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements "CL1", "CK0", and "CK1"); *It should be noted that "CL1" is analogous the "second clock signal" and "CK1" is analogous to the "second pipeline control signal." It should also be noted that when taking the circuits from Figs. 18A and 18B and using those circuits to generate "CK1" as illustrated in Figs. 19A and 19B, the signal "CLK" is replaced with the signal "CL1", as explained in col. 20, lines 61-63.*

a first pipeline stage which latches the data on the data transfer path in response to pulses of the first pipeline control signal (col. 15, lines 45-55; Fig. 8B, elements "S0" and "CK0"); *It should be noted that "S0" is analogous to the "first pipeline stage."*

a second pipeline stage which latches the data latched by the first pipeline stage in response to pulses of the second pipeline control signal (col. 15, lines 45-55; Fig. 8B, elements "S1" and "CK1"); *It should be noted that "S1" is analogous to the "second pipeline stage."*

and a third pipeline stage which outputs the data latched by the second pipeline stage to a data output pad in response to a data output clock signal (col. 15, lines 45-55; Fig. 8B, elements "S2" and "CK2"; Fig. 2, element 21; Figs. 19A and 19B), *It should be noted that when m=2, "S2" is analogous to the "third (and final) pipeline stage" where the data Dout is outputted. It should also be noted that "CK2" is analogous to the "data output clock signal."*

wherein an initial pulse of the second pipeline control pulse signal is delayed relative to an initial pulse of the first pipeline control pulse signal (Fig. 17, elements "CK0" and "CK1"). *It should be noted that "CK2" is delayed relative to "CK1."*

Toda-465 does not disclose a pulse width of at least the initial pulse of the second pipeline control signal is less than a pulse width of each of the pulses of the first pipeline control pulse signal.

Nam discloses a pulse width of at least the initial pulse of the second pipeline control signal is different than a pulse width of each of the pulses of the first pipeline control pulse signal (col. 7, lines 33-37; Fig. 13).

Toda-465 and Nam are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Nam's system of producing control signals with variable pulse widths, which is based on the delays of the respective sets of three inverters connected in cascade within the pulse generating circuit, within Toda-465's internal clock generating circuit such that a pulse width of at least the initial pulse of the CK1 is less than a pulse width of each of the pulses of CK0. The motivation for doing so would have been to output the valid data within the shortest time by generating pipeline control signals of each stage with a minimum margin for possible changes of a temperature and power supply voltage (Nam, abstract).

10. **As per claim 2**, the combination of Toda-465/Nam discloses the data fetching control circuit comprises:

a first edge trigger delay circuit which receives a first clock signal and generates the first pipeline control pulse signal (Toda-465, col. 20, lines 50-53; col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B, elements 29 and 32; Figs. 19A and 19B, elements "CLK/CLK0" and "CK0"); *As noted above, when taking the circuits from Figs. 18A and 18B and using those circuits to generate "CK0" as illustrated in Figs. 19A and 19B, the signal "P1" is always high and the signal "CK0" is a don't care, as explained in col. 20, line 63 - col. 21, line 3. Thus, "CK0" is obtained by buffering "CLK/CLK0" through NAND gates 29 and 32. Accordingly, NAND gates 29 and 32 are analogous to the "first edge trigger delay circuit."*

and a multiplexer which receives a second clock and the first pipeline control pulse signal, and generates the second pipeline control pulse signal (Toda-465, col. 20, lines 41-48 and 54-63; Figs. 18A and 18B, element 32; Figs. 19A and 19B, elements "CL1", "CK0", and "CK1"). *It should be noted that NAND gate 32 receives a buffered version of "CK0" and a buffered version of "CL1" and generates "CK1." Thus, NAND gate 32 is analogous to Applicant's "multiplexer."*

11. **As per claim 3**, the combination of Toda-465/Nam discloses the first edge trigger delay circuit comprises an even number of inverters in a chain (Toda-465, col. 20, lines 50-53; col. 20, line 63 – col. 21, line 3; Fig. 18A, elements 29 and 32). *It should be noted that a NAND gate is logically equivalent to an inverter connected to the output of an AND gate. Thus, NAND gates 29 and 32 are logically equivalent to a first inverter connected to the output of a first AND gate and a second inverter connected to the output of a second AND gate. Accordingly, NAND gates 29 and 32 comprise an even number of inverters (2 inverters) in a chain.*

12. **As per claim 6**, Toda-465 discloses a data fetching method for a pipeline memory device, comprising:

transferring data stored in memory cells along a transfer path (col. 10, lines 38-41 and 50-54; Fig. 1; Fig. 2, element 24);

generating a first pipeline control pulse signal in response to a first clock signal (col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements "CLK/CLK0" and "CK0"); *See the citation note for the similar limitation in claim 1 above.*

generating a second pipeline control pulse signal in response to a second clock signal and the first pipeline control signal (col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements "CL1", "CK0", and "CK1"); *See the citation note for the similar limitation in claim 1 above.*

latching the data to a first pipeline stage on the transfer path in response to pulses of the first pipeline control pulse signal (col. 15, lines 45-55; Fig. 8B, elements "S0" and "CK0"); *See the citation note for the similar limitation in claim 1 above.*

latching the data to a second pipeline stage on the transfer path in response to pulses of the second pipeline control pulse signal (col. 15, lines 45-55; Fig. 8B, elements "S1" and "CK1"); *See the citation note for the similar limitation in claim 1 above.*

and outputting the data from the second pipeline stage to a data output pad in response to a data output clock signal (col. 15, lines 45-55; Fig. 8B, elements "S2" and "CK2"; Fig. 2, element 21; Figs. 19A and 19B). *See the citation note for the similar limitation in claim 1 above.*

wherein an initial pulse of the second pipeline control pulse signal is delayed relative to an initial pulse of the first pipeline control pulse signal (Fig. 17, elements "CK0" and "CK1"). *See the citation note for the same limitation in claim 1 above.*

Toda-465 does not disclose a pulse width of at least the initial pulse of the second pipeline control signal is less than a pulse width of each of the pulses of the first pipeline control pulse signal.

Nam discloses a pulse width of at least the initial pulse of the second pipeline control signal is different than a pulse width of each of the pulses of the first pipeline control pulse signal (col. 7, lines 33-37; Fig. 13).

Toda-465 and Nam are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Nam's system of producing control signals with variable pulse widths, which is based on the delays of the respective sets of three inverters connected in cascade within the pulse generating circuit, within Toda-465's internal clock generating circuit such that a pulse width of at least the initial pulse of the CK1 is less than a pulse width of each of the pulses of CK0. The motivation for doing so would have been to output the valid data within the shortest time by generating pipeline control signals of each stage with a minimum margin for possible changes of a temperature and power supply voltage (Nam, abstract).

13. **As per claim 8**, the combination of Toda-465/Nam discloses the pulses of the second pipeline control pulse signal do not overlap the pulses of the first pipeline control pulse signal (Toda-465, Fig. 17, elements "CK0" and "CK1").

14. **As per claim 9**, Toda-465 discloses an apparatus comprising:

at least one memory cell (col. 10, lines 45-46; Fig. 2, element 12);

a first pipeline stage coupled to the output of the at least one memory cell, wherein the first pipeline stage is driven by a first control pulse signal (col. 15, lines 45-

55; Fig. 8B, elements "S0" and "CK0"); *It should be noted that "S0" is analogous to the "first pipeline stage" and that "CK0" is analogous to the "first control signal."*

and a second pipeline stage coupled to the output of the first pipeline stage, wherein the second pipeline stage is driven by a second control pulse signal (col. 15, lines 45-55; Fig. 8B, elements "S1" and "CK1"; col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements "CK0" and "CK1"); *It should be noted that "S1" is analogous to the "second pipeline stage" and that "CK1" is analogous to the "second control signal."*

wherein an initial pulse of the second pipeline control pulse signal is delayed relative to an initial pulse of the first pipeline control pulse signal (Fig. 17, elements "CK0" and "CK1"). *See the citation note for the same limitation in claim 1 above.*

Toda-465 does not disclose a pulse width of at least the initial pulse of the second pipeline control signal is less than a pulse width of each of the pulses of the first pipeline control pulse signal.

Nam discloses a pulse width of at least the initial pulse of the second pipeline control signal is different than a pulse width of each of the pulses of the first pipeline control pulse signal (col. 7, lines 33-37; Fig. 13).

Toda-465 and Nam are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Nam's system of producing control signals with variable pulse widths, which is based on the delays of the respective sets of three inverters connected

in cascade within the pulse generating circuit, within Toda-465's internal clock generating circuit such that a pulse width of at least the initial pulse of the CK1 is less than a pulse width of each of the pulses of CK0. The motivation for doing so would have been to output the valid data within the shortest time by generating pipeline control signals of each stage with a minimum margin for possible changes of a temperature and power supply voltage (Nam, abstract).

15. **As per claim 10**, the combination of Toda-465/Nam discloses the first control pulse signal and the second control pulse signal are driven by a clock signal (Toda-465, col. 20, line 41 – col. line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements "CLK/CLK0", "CK0", and "CK1"). *It should be noted that external clock signal CLK0 drives CK0 and in turn CK0 drives CK1. Therefore, it follows that external clock signal CLK0 drives CK0 and CK1.*

16. **As per claim 12**, the combination of Toda-465/Nam discloses each pulse of the first control pulse signal is delayed relative to each pulse of the clock signal by a first delay (Toda-465, col. 16, lines 43-46; Fig. 17, elements "CLK" and "CK0"); *It should be noted that CK0 has substantially the same timing as the external clock signal CLK rather than the exact same timing as the external clock signal CLK. Therefore, it follows that CK0 is delayed from CLK by a finite amount of time (even if this amount of time is extremely small).*

and wherein each pulse of the second control pulse signal is delayed relative to each pulse of the clock signal by a second delay (Fig. 17, elements "CLK" and "CK1").

17. **As per claim 14**, the combination of Toda-465/Nam discloses the pulses of the first control pulse signal do not overlap the pulses of the second control pulse signal (Toda-465, Fig. 17, elements "CK0" and "CK1").

18. **As per claim 17**, the combination of Toda-465/Nam discloses the data fetching control circuit comprises a first circuit which generates the first pipeline control pulse signal, and a second circuit which generates the second pipeline control pulse signal (Fig. 19A, elements 24, 35-0, and 35-1),

wherein first circuit of the data fetching control circuit receives a first clock signal and outputs the first pipeline control pulse signal in accordance with the first clock signal (col. 20, line 63 – col. 21, line 3; Figs. 18A and 18B; Figs. 19A and 19B, elements "CLK/CLK0" and "CK0"),

and wherein the second circuit of the data fetching control circuit receives a second clock signal and the first pipeline control pulse signal, and outputs the second pipeline control pulse signal in accordance with the second clock signal and the first pipeline control pulse signal (col. 20, lines 41-48 and 54-63; Figs. 18A and 18B; Figs. 19A and 19B, elements "CL1", "CK0", and "CK1").

**19. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toda-465 and Nam as applied to claim 10 above, and further in view of Toda (U.S. Patent 6,449,727) (hereinafter "Toda-727").**

20. **As per claim 11**, the combination of Toda-465/Nam discloses all the limitations of claim 13 except the clock signal is an internal clock signal.

Toda-727 discloses generating an internal clock signal from an external clock signal (col. 16, lines 5-9).

The combination of Toda-465/Nam and Toda-727 are analogous art because they are from the same field of endeavor, that being memory module systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to convert use Toda-727's internal clock signal generating circuits to convert Toda-465/Nam's external clock signal "CLK" into a master internal clock signal because all the claimed elements were known in the prior art and one skilled in the art could have combined the elements as claimed by know methods with no change in their respective functions, and the combination would have yielded the predictable results of allowing a memory controller to compensate for a difference between the timings of transfer data resulting from a difference between environments such as a difference between the numbers of memory modules. Consequently, high-speed synchronous data transfer is realized.

***Response to Arguments***

21. Applicant's arguments filed September 5, 2008 with respect to **claims 1-3, 6, 8-12, 14, and 17** have been considered but are moot in view of the new grounds of rejection above.

22. Applicant's arguments filed September 5, 2008 with respect to **claim 13** have been fully considered but they are not persuasive.

With respect to Applicant's argument regarding the rejection of claim 13 under 112, first and second paragraphs, which appear on pages 7-8 of the communication filed September 5, 2008, the Examiner respectfully disagrees. The Examiner directs Applicant above to sections the 3-6 of the current Office action which contain the 112, first and second paragraph rejections of claim 13.

The Examiner also notes that the example given by Applicant on pages 7-8 of the communication filed September 5, 2008 is not commensurate with the current language of claim 12. As currently amended, claim 12 recites each pulse of the second control pulse is delayed relative to each pulse of the clock signal by a second delay, however, Applicant's example clearly ignores the delay of the initial second control pulse signal relative to the initial clock signal. (emphasis added) Applicant's example would make sense if in claim 12, each pulse of the first control pulse signal (FRP) is delayed relative to each pulse of the clock signal (PCLK) by a first delay (the left-most arrow in Fig. 7) and the initial pulse of the second control pulse signal (SRP) is delayed relative to the second pulse of the clock signal (PCLK) by a second delay (the second-to-the-left-most arrow in Fig. 7). However, claim 12 does not recite such a feature and therefore claim 13 continues to have problems under 112, first and second paragraphs. Accordingly, the Examiner maintains the 112, first and second paragraph rejections of claim 13.

***Conclusion***

**STATUS OF CLAIMS IN THE APPLICATION**

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

***Allowable Subject Matter***

23. **Claims 4 and 5** are allowed for the reasons appearing in the Office action dated April 21, 2006.

24. **Claim 13** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st and 2nd paragraphs, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

***Claims Rejected in the Application***

25. Per the instant office action, **claims 1-3, 6, 8-14, and 17** have received an action on the merits and are subject of a final action.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Arpan Savla/
Examiner, Art Unit 2185
March 12, 2009

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185